Methodology on power estimation of memory modules with Pseudo-open drain and Center-tab termination type termination schemes

2011. 11
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Contents

- Background
  - Elements in server system

- Power consumption in server system
  - Memory requirements in data center
  - Power consumption in DRAM
  - Termination schemes for DRAM Interface

- Methodology for power estimation of DRAM Interface
  - Signal integrity simulation for DRAM interface
  - Power estimation for DRAM interface
    - Overview
    - Methodology
    - Results

- Closing Remarks
Contents

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■ Closing Remarks
Server system

- CPU
- Memory
- Disk
- Power supply & Others

Components of a server system.
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### Memory requirements in data center

- **Memory is most critical for performance in data center**
  - Many application servers need high performance memory
  - According to cloud computing growth, memory requirement is getting stronger

<table>
<thead>
<tr>
<th>Performance</th>
<th>CPU</th>
<th>Memory</th>
<th>Disk</th>
<th>Network</th>
</tr>
</thead>
<tbody>
<tr>
<td>Web server</td>
<td>🌟🌟</td>
<td>🌟🌟🌟🌟</td>
<td>🌟🌟</td>
<td>🌟🌟🌟🌟</td>
</tr>
<tr>
<td>E-mail Server</td>
<td>🌟🌟🌟</td>
<td>🌟🌟🌟🌟</td>
<td>🌟🌟🌟</td>
<td>🌟🌟🌟🌟</td>
</tr>
<tr>
<td>Database Server</td>
<td>🌟🌟🌟🌟</td>
<td>🌟🌟🌟🌟</td>
<td>🌟🌟🌟</td>
<td>🌟🌟🌟🌟</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power Consumption</th>
<th>20%</th>
<th>26%</th>
<th>2%</th>
<th>52%**</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOM* Portion</td>
<td>25%</td>
<td>50%</td>
<td>10%</td>
<td>15%**</td>
</tr>
</tbody>
</table>

* BOM (Bill Of Material)  
** Others (Network, AC loss, Main board, Etc.)

Source: IBM, DELL, SAMSUNG
**Power consumption in DRAM**

Maintenance cost in data center: a quarter is caused by power.

- Server: 50%
- Power: 23%
- Labor: 15%
- Others: 2%

Source: IDF Beijing 2010

**Power portion in server:** Memory power accounts for main portion on the server system.

- Others: 47%
- CPU: 33%
- DRAM: 30%

Source: Google Data Center, circa 2007

Power consumption in DRAM:

- Total main memory on server system [GB]:
  - 16GB: Others 11%, CPU 49%, Memory 40%
  - 32GB: Others 15%, CPU 47%, Memory 38%
  - 48GB: Others 18%, CPU 45%, Memory 37%
  - 96GB: Others 27%, CPU 41%, Memory 32%

Source: Samsung Lab
Termination schemes for DRAM interface

Elements in Registered DIMM
- Registered DIMM consists of DRAM, active element, passive element
- DRAM has input/output buffer including termination schemes

Registered DIMM
- DRAM
  - Cell & Core
  - IO Buffer
- Active Elements
  - RCD (Registering clock driver)
  - EEPROM
- Passive Elements
  - Resistor, Capacitor
Termination schemes for DRAM interface

Termination schemes in DRAM input/output buffer
- POD (Pseudo-Open Drain) vs CTT (Center Tab Termination)
- CTT consumes more current than POD

**POD**
- Output Driver @ Chipset
- $R_{POD}$
- $Rs$

**CTT**
- Output Driver @ Chipset
- $2*R_{ODT}$
- $2*R_{ODT}$
- $R_{s}$
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Signal integrity simulation for DRAM interface

- **Signal integrity comparison**
  - CTT and POD have little difference in Skew and Aperture

<table>
<thead>
<tr>
<th>Condition: Write operation with 34ohm linear driver</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1DPC</strong></td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td><strong>1600 Mhz</strong></td>
</tr>
<tr>
<td><strong>1866 Mhz</strong></td>
</tr>
<tr>
<td><strong>2133 Mhz</strong></td>
</tr>
</tbody>
</table>
Overview

- Concept of power estimation

Power estimation for DRAM interface

DRAM with POD turned-on

Chipset

**Overview**

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DRAM with POD turned-on

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Power estimation for DRAM interface

Flow chart for estimation

- Start
- Characteristics
  - Capacitance in IO buffer, PCB trace
  - Resistance in output driver
- Termination condition
  - VDD, termination value
- Data output
  - Data ‘0’ : ‘1’ portion
- System condition
  - Write : Read portion
  - Bus efficiency
  - Operation frequency
- Estimation result
  - Consider variables
  - Use estimation methodology
# Methodology

- Estimation considers every case in which POD consumes power
- POD (Pseudo-Open Drain) consumes power all cases except when it remains Stay ‘1’

**Average DRAM power consumption @POD**

\[ \frac{3 \times Pd0 + 2 \times Pdt}{8} \]

**POD** : Staying, **Pdt** : Transition

\[ Pd = \frac{\Delta V^2}{R_{POD}} \]
**Estimation Result**

- **POD** (Pseudo-Open Drain) consumes less power than **CTT**.
- **POD** is suitable for IO termination scheme of DDR4.

<table>
<thead>
<tr>
<th>Speed (Mhz)</th>
<th>POD(X72)</th>
<th>CTT(X72)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1333</td>
<td>239.3</td>
<td>732.8</td>
</tr>
<tr>
<td>1600</td>
<td>240.3</td>
<td>743.9</td>
</tr>
<tr>
<td>1866</td>
<td>241.1</td>
<td>752.3</td>
</tr>
<tr>
<td>2133</td>
<td>241.7</td>
<td>759.0</td>
</tr>
</tbody>
</table>

Unit: mW
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Summary

- **Power consumption in server system**
  - Main memory accounts for 20~30% in the server system
  - Termination schemes are applied in DRAM interface
    - POD (Pseudo-Open Drain) & CTT (Center Tab Termination)

- **Methodology for power estimation of DRAM Interface**
  - In signal integrity simulation for DRAM interface
    - CTT and POD have little difference in skew and aperture
  - In power estimation for DRAM interface
    - POD (Pseudo-Open Drain) consumes less power than CTT
    - POD is suitable for IO termination scheme of DDR4
Align with your imagination

Thank you